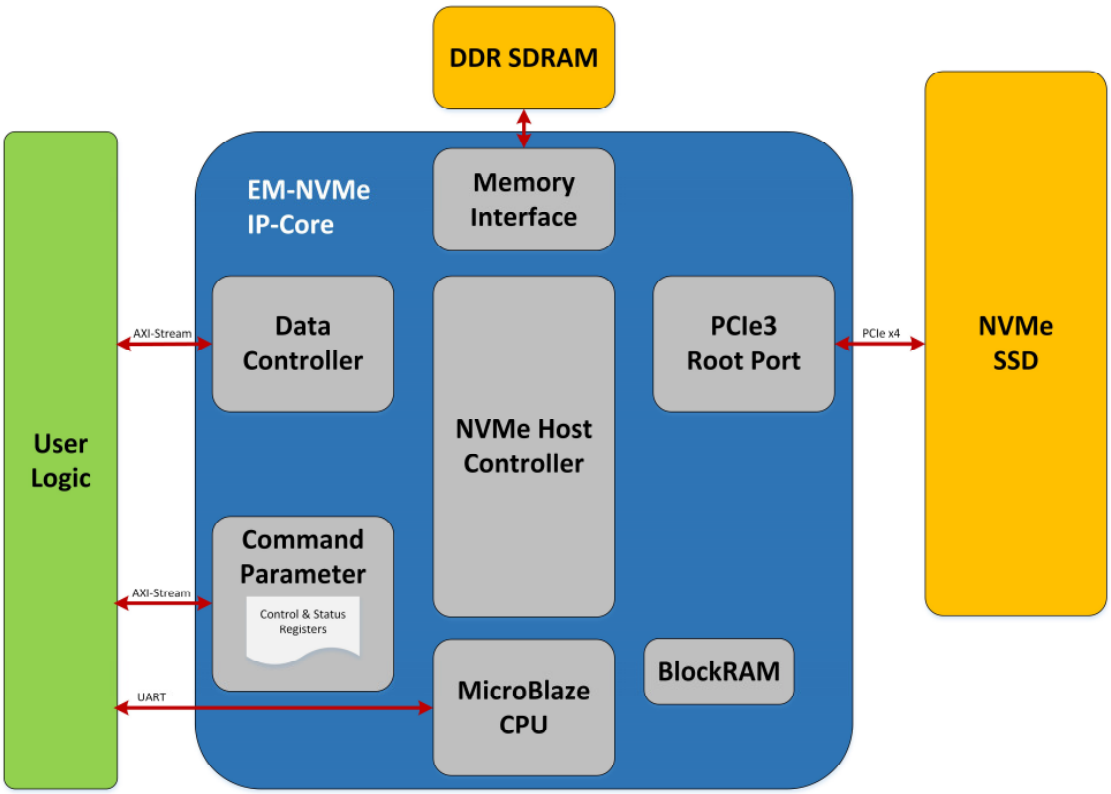
EM-NVMe IP-Core

NVMe Host Controller with PCIe Root Complex



NVMe Host Controller IP-Core for Xilinx Series 7 and Ultrascale FPGAs

- For FPGA applications with high-speed storage requirements
- AXI Streaming interface to access NVMe via PCIe x4 Gen.3
- PCIe Root Complex on FPGA / internal CPU
- No external CPU needed
- Vivado project (Vivado 2018.1)
- VHDL, Verilog and System Verilog source code
- Example and test design to validate the NVMe Subsystem
- Reference implementation on MicroTCA system with Virtex 7 690 T
- Customization for other Hardware platforms available

EM-NVMe IP-Core is an IP-Core for Xilinx Series 7 and Ultrascale FPGAs that the supports the direct access to NVMe Storage via PCIe x4. It is perfectly suited for FPGA applications that need a high-speed access to flash storage without an external CPU.

The NVMe Subsystem is delivered as multiple (toplevel and sub-cores) packaged IP-Xact IP Cores for Xilinx Vivado 2018.1.

FPGA Design

The User Logic Interface is provided via AXI4-Streaming for Sending and Receiving of NVMe data. An AXI4-Lite Slave is used for accessing control and status registers.

The Xilinx AXI Bridge for PCI Express Gen3 IP is used to enable connectivity to the PCIe hierarchy as Root Complex.

The NVMe Host Controller IP performs memory transfers to or from the NVMe storage, controlled by embedded software.

Embedded Software

Implemented as standalone MicroBlaze application as part of the EM-NVMe IP-Core.

Supports PCIe enumeration and NVMe initialisation. It controls the data transfer between user logic AXI4 -Stream interfaces and NVMe SSD. Data transfer is handled directly by the FPGA.

Provides logging output via FPGA internal UART and polling of various status indicators in the AXI4-Lite accessible status registers.

Example and Test Design

A Vivado 2018.1 example and test design is provided for reference. It is implemeted on a MicroTCA FPGA FMC carrier board AMC525 with Xilinx Virtex 7 690T and external PCIe x4 Gen.3 connection to an M.2 NVMe carrier board.

It instantiates the NVMe Subsystem in HDL and includes an additional block design with MicroBlaze processor for testing the NVMe Subsystem. Software output is provided via the Xilinx JTAG UART. The four AMC525 LEDs are used to signal the status of the NVMe IP-Core.

Ordering Information

Configuration	Description	Order Code
EM-NVMe IP-Core	NVMe Host-Controller IP-Core for Xilinx Series 7 and Ultrascale FPGAs	**A09176**

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